



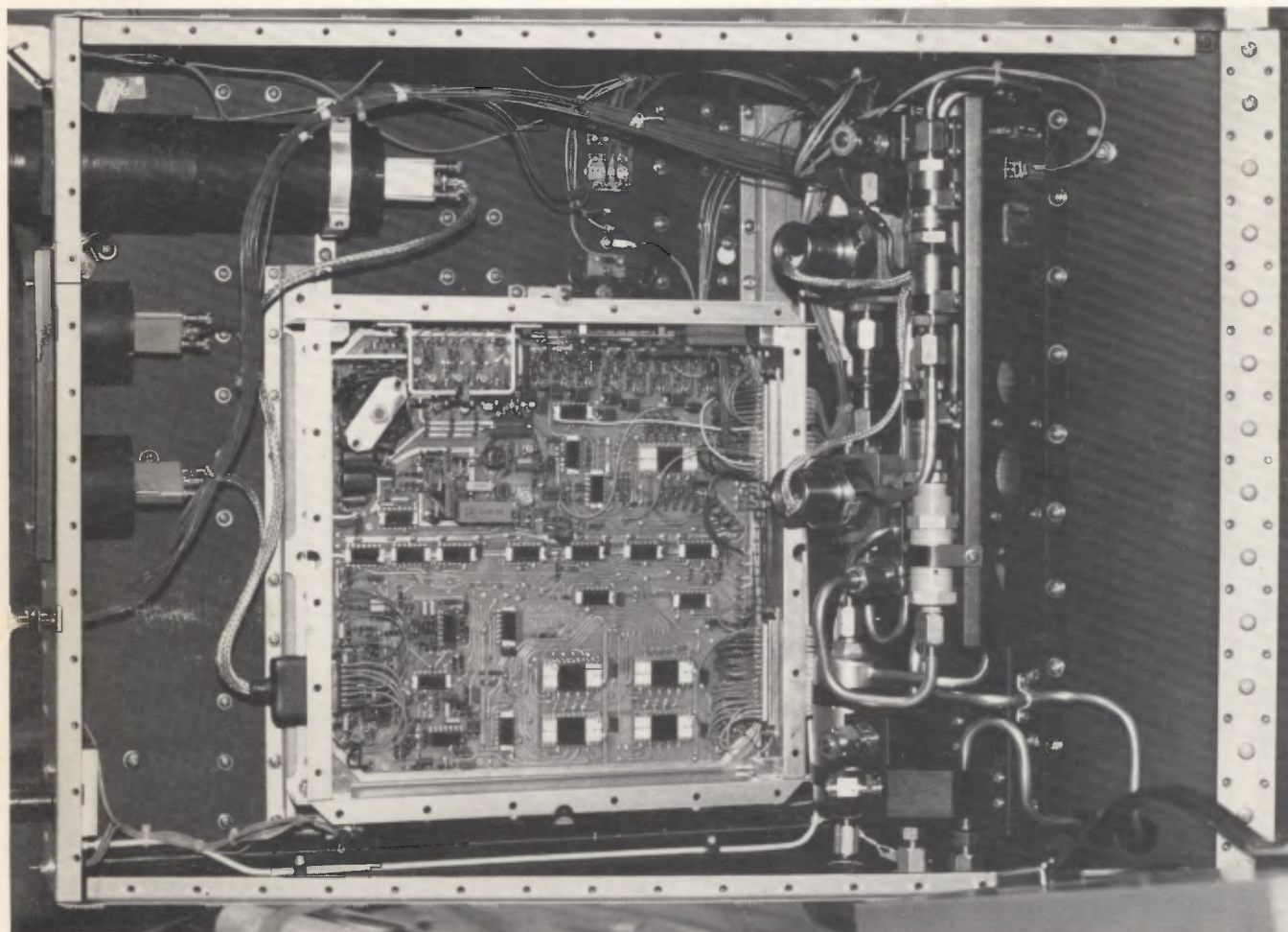
AMSAT-NA **Technical Journal**

Volume 1, No. 1

Summer, 1987

A Look at the Phase-3C Spacecraft

Pages 13-14



AMSAT-NA Technical Journal

AMSAT-NA Technical Journal is a publication of the Radio Amateur Satellite Corporation of North America, AMSAT-NA. *AMSAT-NA Technical Journal* publishes papers reporting original work and significant findings in the fields of low-cost satellite design, construction, and operation, space communications, space sciences and related social value issues.

Contributions to *AMSAT-NA Technical Journal* are unrefereed working papers. Their content should be considered the personal opinion of the authors rather than organizational (company, any AMSAT group, etc.) unless otherwise noted. Readers who may wish to express their opinion on the content of an article may contact the author or the editor will forward their comments to the author.

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Material for publication should be submitted both in hardcopy form and as a text file on diskette. Any 5¼ inch format is acceptable provided the format is clearly indicated and all special character sequences used by word processors have been deleted from the text file. Figures should be drawn in a manner suitable for publication and larger than the size in which they will appear when published.

All material submitted to the Editor will be considered for publication unless otherwise requested. No material will be returned. A contribution to *AMSAT-NA Technical Journal* is welcomed from any person with an interest in the amateur radio space program. Contributions should be sent to:

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AMSAT-NA Technical Journal is published twice yearly in June and November for \$10 by AMSAT, 850 Sligo Ave., Suite 601, Silver Spring, MD 20910. POSTMASTER: Send address changes to *AMSAT-NA Technical Journal*, 850 Sligo Ave., Suite 601, Silver Spring, MD 20910.

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On the cover: Phase 3-C spacecraft.

Left side: Top large black tube, earth sensor.
Next two lower units, sun sensors.

These sensors provide input to the sensor electronics unit and the onboard computer in order to determine the attitude of the spacecraft in orbit.

Center: Sensor electronics unit module.

The SEU accepts input from the earth and sun sensors and processes it in conjunction with the onboard computer.

Right side: Propellant flow assembly.

The propellant flow assembly controls the flow of the fuel and oxidizer to the kick motor under control of the onboard computer and the liquid ignition unit.

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President's Message

AMSAT is privileged to have among its members some of the brightest minds in amateur radio and some of the best talent anywhere. Having brains and talent in an organization is one thing. Harnessing it and converting these assets to action and achievement is quite another matter. The key ingredient to harnessing brains and talent, I've learned, is instilling a communications discipline; a yearning to share ideas and concepts with others to promote growth and cross-pollenization.

A few years ago it became obvious to me we were collectively inadequate in communicating the ideas of the best and the brightest among us. This first edition of ATJ redresses that inadequacy in a significant first step.

When I asked Editor Bob Diersing to undertake this assignment, he promised to do his best. The result speaks for itself. Congratulations to Editor Diersing and the fine authors who have shared these excellent papers with us. My fondest hope and desire is that this edition should be but the first of a long series documenting the significant contributions made by the authors and their colleagues. Moreover, this record will illustrate the extent to which AMSAT has contributed to the advancement of amateur radio and ultimately to society at large whose spectrum we use in pursuit of our technical wizardry.

Vern Riportella, WA2LQQ, President
June 1, 1987

Editorial

by

Robert J. Diersing, N5AHD
Associate Professor of Computer Science
Corpus Christi State University

Introduction

This first issue of *AMSAT-NA Technical Journal* has been in the making for a little more than a year—since March of 1986. As many of you know, the idea was conceived even earlier with the first call for papers having been published in April of 1985. It has taken longer than I hoped to get the first issue in circulation. However, upon reflection, a little more than a year from the time the first material was in hand to final production is not unrealistic.

I will take the liberty to write a longer than usual editorial because there are a variety of topics to be addressed. First, I will review some of the objectives for ATJ. Next will be some commentary on the articles that have been published. Finally, those who have contributed to this issue will be recognized including those who have worked behind the scenes.

AMSAT-NA Technical Journal Objectives

Many professional organizations produce a multitude of technical publications. Large organizations such as the Institute of Electrical and Electronic Engineers (IEEE) and the Association for Computing Machinery (ACM) have at least one technical publication for each special interest group within the respective societies. These publications document the state-of-the-art theoretical and applied work done by the leaders in the fields they represent. For the most part, the very serious work done by AMSAT-NA members has gone undocumented.

Long-time AMSAT members will easily recognize the differences between this publication and both past and current AMSAT publications. A goal of *AMSAT-NA Technical Journal* is to make spacecraft users aware of the tremendous technological challenge associated with the design, construction and operation of modern amateur radio satellites. More importantly, it will be an absolute necessity that this work be documented for certain sources of funds to be exploited for projects like Phase-4.

It is recognized that much of the material presented in these pages cannot be considered easy reading. It is hoped that curiosity will bring satellite users to read ATJ. Speaking from personal experience, I cannot say that I have ever advanced in a technical field without studying material that was completely beyond my level of experience at the time. During the past several years I have participated in a number of forums at ham conventions in Texas. One question that is always asked is, "when are you going to build a geostationary satellite?" Hopefully, ATJ will contain articles describing the engineering considerations for building all types of

amateur radio spacecraft.

Finally, and equally important, we hope to bring you articles from our AMSAT colleagues around the world. This goal is apparent in this issue. With the current level of satellite design and construction activity around the world, articles for future issues of ATJ should be in abundance. Just as amateur radio itself is an international fraternity, so is the group of people who have chosen to specialize in satellite construction and operation. Even when the satellite is primarily the product of a single nation, the technology developed should benefit all AMSAT engineering and user groups.

Contents of this Issue

Consistent with the fact that the first issue should set the tone for future issues, I have tried to include material covering the areas of design, construction and operation. At the same time, I have tried to have activities of several countries represented.

Every spacecraft construction project begins with a conceptual design which must later be refined. Two articles related to the proposed Packet Technology Satellite Experiment-Houston (PTSE-H) project have been included. Gerry Creager, N5JXS, presents the general concepts of the proposed spacecraft. Courtney Duncan, N5BF, shows some of the details of selecting an orbit and spacecraft attitude that will generate enough power for onboard systems.

Since conception and launch of UoSAT-1 in October of 1981, the University of Surrey has been engaged in research in all areas of cost-effective spacecraft engineering and operation. Jeff Ward, G0/K8KA, provides an analysis of the performance of the different types of memory used in the UoSAT-2 Digital Communications Experiment (DCE). Data gathered from experiments such as the DCE is valuable not only to those building amateur radio satellites but to commercial builders as well.

With the launch of Phase-3C still in the future, three articles have been included from our colleagues at AMSAT-DL. Two of them are related to the AFREG 400 bit/s telemetry data demodulator—one describes the operation of the unit and the other gives the alignment procedure. Another article describes a BPSK modulator of the type required for the RUDAK uplink. Finally, Bob McGwier, N4HY, gives the theoretical development of the algorithm used in the Quicktrak program. These four articles show the hardware and software engineering that must be done to support spacecraft in orbit and eventually the amateur satellite enthusiast as end user.

Acknowledgements

I would like to thank all who submitted articles for this premier issue of *AMSAT-NA Technical Journal*. If you submitted an article and it was not published don't give up hope—this is not the last issue. I did not go through this learning process to give up after one issue.

Special thanks go to the authors outside the United States for persevering through the obstacles of working with an editor an ocean away. Werner Haas, DJ5KQ, of AMSAT-DL provided the material that has been reprinted from *AMSAT-DL Journal*. We will be including more articles from AMSAT-DL in the future, especially on RUDAK. Jeff Ward, G0/K8KA, at the University of Surrey also put forth the extra effort to meet my constantly vague deadlines.

Many others have contributed to this publication. The person who has done the most to insure that ATJ

Volume 1, Number 1 made it to press is John Stalmach of the Corpus Christi State University Office of Public Information. John has been a one-man production team and even agrees to do another issue! Text entry and proofreading at many stages was done by my former secretaries Maureen Brown and Ruth Killins. No, they didn't quit because of this project.

I would also like to recognize my wife Julie, the ultimate proofreader. The trained eye of an English/business major who teaches typing is hard to beat. One of her comments along the way was, "I don't know what a magnetorquer is but I don't think it should be spelled three different ways."

Finally, thanks to AMSAT-NA President Vern Riportella, WA2LQQ, for the encouragement and patience required to begin a new project and see it to completion.

An Analysis of UoSAT-2 DCE Memory Performance

by Jeff W. Ward, G0/K8KA

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ABSTRACT

The Digital Communications Experiment payload on UoSAT-2 (OSCAR-11) was designed to provide both a facility for Amateur Radio digital communications and a test vehicle for the hardware and software necessary for large-scale store-and-forward satellite communications. The hardware is being monitored for permanent memory failures, temporary memory upsets and long-term changes in power consumption. This paper presents data gathered during 1985 and 1986 along with some preliminary conclusions drawn from that data.

1.0. The Digital Communications Experiment

The UoSAT-2 mission (conceived in 1983 for 1984 launch) gave several groups of experimenters outside of the University of Surrey the opportunity to get payloads into orbit. One of these groups was the North American AMSAT group working on PACSAT [1]. Early design work for PACSAT had already been done, and flying a small store-and-forward transponder on UoSAT-2 was an ideal opportunity to test hardware and software for use in a dedicated PACSAT satellite.

The resulting small, low-power payload, which was designed, built and tested in only a few months, is the UoSAT-2 Digital Communications Experiment (DCE). The DCE is a store-and-forward communications module built around an NSC-800 microprocessor and 126 kbytes of RAM. It has two asynchronous communications ports which can be connected to any of the UoSAT-2 RF communication channels or the On-Board Computer (OBC).

UoSAT-2 was launched on March 1, 1985 (becoming UoSAT-OSCAR-11), and the DCE was activated in June 1984 to provide an emergency communications link for command of UoSAT-2. A complete store-and-forward operating software system, called MSG2, was put into operation early in 1986, and has seen daily use since then. The structure of MSG2, and details of the use of the DCE to relay Amateur Radio communications are discussed in detail in [2]. The DCE has proven that store-and-forward digital communications from a small satellite to small groundstations is technically viable. But the DCE has another important goal to achieve—the space testing of microcomputer and memory ICs that will be needed to build larger store-and-forward satellite communications systems.

2.0. DCE Hardware

The DCE hardware was designed to meet both the operational and the experimental goals of the payload. The microprocessor, the RAMs and all of the I/O chips are CMOS ICs, resulting in low power consumption which allows the DCE to operate continuously. An NSC-800 processor was chosen because AMSAT had no flight experience with it, and because common Z-80 software development systems can be used to develop code for the NSC-800. UARTs were chosen for I/O because CMOS ICs capable of handling the HDLC protocol were not available, and development time was too short to build an HDLC controller in discrete components (as was done for FO-12).

To provide a wide range of experience with the radiation tolerance and soft-error characteristics of CMOS RAMs, RAMs of several sizes from several makers were used. While this hardware is well-described in [2] and [3], it is important here to clarify the distribution of the memories both within the DCE memory map and on the three PC boards which make up the DCE.

2.1. Memory Map

The DCE memory map is shown in Figure 1. The memory is distributed among three PC boards: the CPU board, the General Memory (GMEM) board and the RAM Unit board. The GMEM board and RAMUNIT board contain only memory ICs and the associated selection and buffering devices. The CPU board also includes the two UARTS, the parallel I/O chip, and the system clock.

2.1.1. PROM

At the bottom of memory (0000-01FF) is the 512-byte Harris 6641 PROM containing the DCE bootloading program. This is a fusible link PROM, and it is provided with an identical backup device. The primary device is functioning correctly, with the bootloader being used to upload all MSG2 software. There has been no need to use the redundant backup. PROM is the only memory on the CPU board.

2.1.2. Harris 2k X 8

Between addresses 07FF and 3FFF are 7 Harris 6564 2k X 8 bit CMOS static RAMS. This is the "general memory" on the GMEM board. Being high-density ICs, these chips are not provided with error detection and correction (EDAC) hardware.

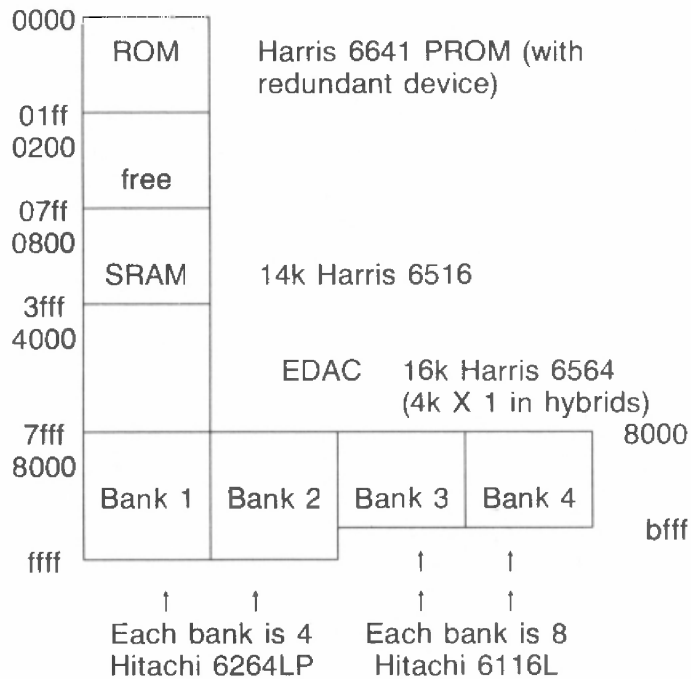


Figure 1. DCE Memory Map

2.1.3. Harris 16k X 4

DCE programs run in the 16 kbytes of memory between 4000 and 7FFF. This is provided by three Harris 6564 ICs. The 6564s are 16k X 4 bit hybrids, each containing 16 4k X 1 memories. Three 6564s are used to provide a 16k X 12 bit memory area; each 8-bit data byte is stored along with 4 bits of Hamming code EDAC information. This Hamming code is a single-bit error correction code. HCMOS EDAC circuits detect, correct and count errors. The EDAC memory and support circuits are on the GMEM board.

2.1.4. Bank-Switched RAM

Current PACSAT plans call for between 4 and 10 Mbytes of RAM to be used for message storage. One method of providing this much memory in the address space of an 8-bit microprocessor is to use bank switching. In the DCE, 96k of RAM on the RAMUNIT board is divided into 4 banks, each of which can be switched into the addresses between 8000 and FFFF. Banks one and two are 32 kbytes, each using 4 Hitachi 6264LP (8k X 8) CMOS static RAMs. Banks three and four are 16 kbytes of Hitachi 6116L (2k X 8) CMOS statics. These RAMs, and the bank switching hardware are on the RAMUNIT board. Banks are selected using the 82C55 parallel port on the CPU board.

3.0. Telemetry

Each of the three PC boards which make up the DCE has a current monitor, the output of which is sampled by the UoSAT-2 telemetry system. The telemetry system, being critical to the mission, is implemented in radiation-tolerant discrete CMOS logic. It periodically samples 60 analogue channels (voltages, currents, and temperatures) and 100 digital status points, formats this information

into checksummed telemetry frames, and transmits the frames. With the telemetry output running at 1200-bits/sec, each channel is sampled once every 4.84 seconds. Telemetry frames can be monitored directly on the UoSAT-2 downlink, or sent to the On-Board Computer (OBC) for further processing. To provide monitoring of telemetry when the satellite is out of range of the UoS groundstation, the OBC can be instructed to take Whole Orbit Data surveys (WOD). Using the standard 4.84 second sample period and 16 kbytes of the OBC memory, a WOD survey results in just under 19 channel-hours of stored telemetry. The OBC can be instructed to survey any combination of telemetry channels. (For extensive discussion of WOD reception and decoding, see [4] and [5].)

3.1. EDAC Counter

Each time the CPU writes a byte in the EDAC memory, the appropriate Hamming error-correction code is calculated and stored along with the data byte. When bytes are read from the EDAC memory, the Hamming bits are used to detect any errors. If an error is detected, the corrected data byte is placed on the data bus and the EDAC counter is incremented. The corrected byte is not automatically re-stored in the memory, and if an erroneous byte is read several times, the EDAC counter will increment accordingly. The stored byte is only corrected when data is read from a location and then explicitly written back to that location. To make sure that a single error is not counted several times before being corrected permanently by a write operation, the DCE MSG2 software includes a memory "washing" routine which periodically reads and writes each location in EDAC RAM. This routine also monitors the error counter as it reads, and if an error is detected, the location of the error is stored in a special DCE message for downloading. To provide an easily received soft-error rate measurement, the DCE EDAC count is transmitted periodically during normal UoSAT-2 DIARY operations. [2]

3.2. Experiments

Using the EDAC counter, the current sensors on the DCE boards, the temperature sensor on an adjacent payload, special programs for the DCE, and the data collection facilities provided by the 1802 OBC, three distinct experiments are being carried out using the DCE hardware:

- 1) Measuring the rate of occurrence of cosmic-ray induced transient errors in the EDAC RAM.
- 2) Logging and characterizing permanent failures in any of the DCE circuits.
- 3) Monitoring the long-term current consumption characteristics of CMOS RAMs and support circuits.

Experimental data collected since late 1985 is presented here along with some preliminary conclusions and plans for further work.